(Pages : 2) **4693**

Reg. No. : .....

Name : .....

Fifth Semester B.Tech. Degree Examination, September 2014
(2008 Scheme)
(Special Supplementary)
08.503 : COMPUTER ORGANIZATION AND ARCHITECTURE (TA)

Time : 3 Hours Max. Marks : 100

PART – A

Answer **all** questions. **Each** question carries **4** marks.

1. What are the different classes of instructions in MIPS ? Explain.
2. Compare RISC and SISC machines.
3. Define CPU performance. How is CPU performance measured ?
4. What are the different addressing modes in MIPS ? Explain briefly.
5. Briefly explain how ALU control is implemented.
6. What is microprogrammed control ?
7. Differentiate structural hazards and control hazards.
8. What do you mean by locality of reference ? What are the two types of locality ?
9. Write a note on LRU replacement algorithm.
10. What are the steps involved in handling an interrupt ?

P.T.O.

PART – B

Answer **any two** questions from **each** Module. **Each** question carries **10** marks.

Module – I

11. Explain how floating-point numbers are represented in computer's memory. Write a note on floating-point multiplication.

12. Explain the working of restoring integer division hardware with a suitable block diagram and an example.

13. Using Booth's algorithm, multiply 0001110 and 0010011. **(10×2=20 Marks)**

Module – II

14. Explain the single data path in operation for a LW instruction.

15. Explain the multicycle datapath implementation with the help of a block diagram.

16. Write notes on the following :
    i) Pipelining.
    ii) Dynamic branch prediction. **(10×2=20 Marks)**

Module – III

17. Explain the following :
    i) Direct mapped cache
    ii) Fully-associative cache
    iii) Set-associative cache.

18. Explain how a virtual address is mapped to a physical address in virtual memory. What is the role of TLB in address translation ?

19. With the help of a neat block diagram, explain the internal architecture of 8086 microprocessor. **(10×2=20 Marks)**